CODE-PROGRAMMABLE FIELD-PROGRAMMABLE ARCHITECTURALLY-SYSTOLIC REED-SOLOMON BCH ERROR CORRECTION DECODER INTEGRATED CIRCUIT AND ERROR CORRECTION DECODING METHOD

ABSTRACT

A programmable error-correction decoder embodied in an integrated circuit and error correction decoding method that performs high-speed error correction for digital communication channels and digital data storage applications. The decoder carries out error detection and correction for digital data in a variety of data transmission and storage applications. The decoder has three basic modules, including a syndrome computation module, a Berlekamp-Massey computation module, and a Chien-Forney module. The syndrome computation module calculates syndromes which are intermediate values required to find error locations and values. The Berlekamp-Massey module implements a Berlekamp-Massey algorithm that converts the syndromes to intermediate results known as lambda (Λ) and omega (Ω) polynomials. The Chien-Forney module uses modified Chien-search and Forney algorithms to calculate actual error locations and error values. The decoder can decode a range of BCH and Reed-Solomon codes and shortened versions of these codes and can switch between these codes, and between different block lengths, while operating on the fly without any delay between adjacent blocks of data that use different codes. Translator and inverse-translator circuits are employed that allow optimal choice of the internal on-chip Galois field representation for maximizing chip speed and minimizing chip gate count by making possible the use of a novel quadratic-subfield modular multiplier and a novel power-subfield integrated Galois-field divider. A simplified Chien-Forney algorithm is implemented that requires fewer computations to determine error magnitudes for Reed-Solomon codes with offsets compared to conventional approaches, and which allows the same circuitry to be used for different codes with arbitrary offsets.